REMARKS

In the Office Action, the Examiner noted that claims 1, 3-6, 8-16, and 18-23 are pending in the application. The Examiner rejected claims 1, 3-6, 8-16, and 18-23. In view of the above amendments and the following discussion, the Applicants submit that none of the claims now pending in the application are obvious under the provisions of 35 U.S.C. §103. Thus, the Applicants believe that all of these claims are now in condition for allowance.

I. Rejection Of Claims Under 35 U.S.C. §103

A. Claims 1, 4-6, and 19-21

The Examiner rejected claims 1, 4-6, and 19-21 as being unpatentable over Mahajan (United States patent 6,618,358, issued September 9, 2003) in view of Peace (United States patent 6,687,260, issued February 3, 2004) and further in view of Hashiguchi (United States patent 5,987,540, issued November 16, 1999). The Applicants respectfully traverse the rejection.

As discussed in greater detail below, the Applicants submit that Mahajan, Peace, and Hashiguchi, either alone or in combination, do not disclose or suggest at least "wherein each of the plurality of clock based functionalities performs processing of one of the first serial data and the second serial data in accordance with a clock chosen from among the first recovered clock, the second recovered clock and the reference clock" as recited in claim 1. In addition, for similar reasons, independent claims 6 and 19 are also patentable over the cited references.

Mahajan teaches a method and apparatus for switching a clock source from among multiple T1/E1 lines. More specifically, Mahajan teaches a network access server (NAC) that recovers clock signals from incoming T1/E1 lines. A demultiplexor in the NAC selects and outputs one of the recovered clock signals, which is then used to drive the internal data bus of the NAC.

The Examiner acknowledges in the Office Action that "Mahajan et al. do not expressly teach: serial data; a plurality of clock based functionalities; each of the plurality of clock based functionalities performs processing of one of the first serial data and the second serial data in accordance with a clock chosen from among the

first recovered clock, the second recovered clock, and the reference clock" (Office Action, Page 3). The Examiner submits, however, that "Peace discloses: serial data" (Office Action, Page 3) and that "Hashiguchi teaches a plurality of clock based functionalities using a selected clock, for subsequent processing of serial data" (Office Action, page 4), and that these features, in combination with Mahajan, render the Applicants' claims obvious. The Applicants respectfully disagree.

Peace teaches an apparatus and method for flow control of non-isochronous data. One component of this apparatus is an I/O processor that "suitably converts the multi-bit data [of incoming signals] into a serial format and provides the serial data to [a] channel processor" (See Peace, column 4, lines 54-56).

Peace, however, does not teach each and every element of Applicants' independent claims 1, 6, and 19. Namely, Peace, like Mahajan, does not teach or suggest that the entity that processes the serial data (*i.e.*, the I/O processor) is also configured to select from among the recovered clock signals. (*See*, *e.g.*, Applicants' Specification, at least at paragraphs 0055-0056; FIGs. 5-8, where the programmable logic fabric including the clock based functionalities receives both serial data streams for processing and a plurality of clocks (*i.e.*, recovered clocks and a reference clock) from among which to choose for the processing of the serial data streams). In contrast, the I/O processor taught by Peace, which the Examiner appears to equate with the claimed "clock based functionality," merely processes serial data but does not select a clock from among recovered clocks for use in the processing. Peace does not describe or illustrate a component for selecting a clock, much less teach or even imply that the same component that processes the serial data (*i.e.*, the I/O processor) also performs this function.

Hashiguchi teaches a system having a clock signal generating circuit for selectively generating requested clock signals. One component of this system is an output clock selector "for selectively supplying serial clock signals from [a] serial clock generator to a plurality of transmission circuits and a plurality of reception units" (See Hashiguchi, column 6, lines 55-58).

Hashiguchi, however, does not teach each and every element of Applicants' independent claims 1, 6, and 19. Namely, Hashiguchi, like Mahajan, does not disclose

that a reference clock is one of the clock signals from among which the output clock selector may choose. (*See*, *e.g.*, Applicants' Specification, at least at paragraphs 0055-0056; FIGs. 5-8, where the programmable logic fabric including the clock based functionalities receives both recovered clocks and a reference clock from among which to choose for the processing of the serial data streams). By contrast, Hashiguchi only teaches that the serial clock signals generated by the serial clock generator are available for selection by the output clock selector. *See*, for example, FIG. 3 of Hashiguchi, which clearly illustrates that the only clock signals input to the output clock selector come from the serial clock generator. Although the clock signals are generated by the serial clock generator on the basis of a reference clock signal, the reference clock signal is not available to the output clock selector as an option for selection.

Peace and Hashiguchi thus fail to bridge the acknowledged gaps in the teachings of Mahajan. Since none of Mahajan, Peace, and Hashiguchi teaches or suggests a component (*e.g.*, a clock based functionality of a logic fabric) that both processes serial data from a serial bit stream and selects a clock from among a plurality of clocks (*i.e.*, recovered clocks and a reference clock) to use for the processing of the serial data, Mahajan in view of Peace and further in view of Hashiguchi does not teach or suggest each and every element of the Applicants' independent claims 1, 6, and 19. Accordingly, the Applicants contend that independent claims 1, 6, and 19 are patentable over the combination of Mahajan, Peace, and Hashiguchi and, as such, fully satisfy the requirements of 35 U.S.C. §103.

Furthermore, claims 4-5 and 20-21 depend from claims 1 and 19, respectively, and recite additional features. Since Mahajan in view of Peace and further in view of Hashiguchi does not teach or suggest Applicants' invention as recited in independent claims 1 and 19, dependent claims 4-5 and 20-21 are also patentable and are allowable. Therefore, the Applicants contend that claims 1, 4-6, and 19-21 are patentable over Mahajan in view of Peace and further in view of Hashiguchi and, as such, fully satisfy the requirements of 35 U.S.C. §103.

B. Claim 3

The Examiner rejected claim 3 as being unpatentable over Mahajan in view of Peace and Hashiguchi and further in view of Tang (US Publication No. 2002/0075981). The Applicants respectfully traverse the rejection.

As discussed above, Mahajan in view of Peace and further in view of Hashiguchi does not teach or suggest Applicants' invention where a component both processes serial data from a serial bit stream and selects a clock from among a plurality of clocks (*i.e.*, recovered clocks and a reference clock) to use for the processing of the serial data. This deficiency is not bridged by the teaching of Tang.

Therefore, Applicants contend that claim 3 is patentable over the combination of Mahajan, Peace, Hashiguchi, and Tang and, as such, fully satisfies the requirements of 35 U.S.C. §103.

C. Claims 10-12 and 22-23

The Examiner rejected claims 10-12 and 22-23 as being unpatentable over Mahajan in view of Hashiguchi. The Applicants respectfully traverse the rejection.

As discussed above, neither Mahajan nor Hashiguchi teaches or suggests Applicants' invention where a component both processes serial data from a serial bit stream and selects a clock from among a plurality of clocks (*i.e.*, recovered clocks and a reference clock) to use for the processing of the serial data, as claimed in the Applicants' independent claims 10, 22, and 23.

Furthermore, claims 11-12 depend from independent claim 10 and recite additional features. Since Mahajan in view of Hashiguchi does not teach or suggest Applicants' invention as recited in independent claim 10, dependent claims 11-12 are also patentable and are allowable. Therefore, the Applicants contend that claims 10-12 and 22-23 are patentable over Mahajan in view of Hashiguchi and, as such, fully satisfy the requirements of 35 U.S.C. §103.

D. Claim 13

The Examiner rejected claim 13 as being unpatentable over Mahajan in view of Hashiguchi and further in view of Peace. The Applicants respectfully traverse the rejection.

As discussed above, none of Mahajan, Hashiguchi, and Peace teaches or suggests Applicants' invention where a component both processes serial data from a serial bit stream and selects a clock from among a plurality of clocks (*i.e.*, recovered clocks and a reference clock) to use for the processing of the serial data, as recited in the Applicants' independent claim 10.

Therefore, Applicants contend that dependent claim 13 which depends from independent claim 10, is patentable over the combination of Mahajan, Hashiguchi, and Peace, and, as such, fully satisfies the requirements of 35 U.S.C. §103.

E. Claims 14-16 and 18

The Examiner rejected claims 14-16 and 18 as being unpatentable over Mahajan in view of Hashiguchi and further in view of Mann (United States patent 5,251,210, issued October 5, 1993). In response, the Applicants have canceled claim 15 without prejudice. The remainder of the rejection is respectfully traversed.

As discussed above, Mahajan and Hashiguchi both fail to teach or suggest Applicants' invention where a component both processes serial data from a serial bit stream and selects a clock from among a plurality of clocks (*i.e.*, recovered clocks and a reference clock) to use for the processing of the serial data, as recited in the Applicants' independent claim 14. This deficiency is not bridged by the teaching of Mann.

Furthermore, claims 16 and 18 depend from independent claim 14 and recite additional features. Since Mahajan in view of Hashiguchi and further in view of Mann does not teach or suggest Applicants' invention as recited in independent claim 14, dependent claims 16 and 18 are also patentable and are allowable. Therefore, the Applicants contend that claims 14, 16 and 18 are patentable over Mahajan in view of Hashiguchi and further in view of Mann and, as such, fully satisfy the requirements of 35 U.S.C. §103.

F. Claims 8-9

The Examiner rejected claims 8-9 as being unpatentable over Mahajan in view of Peace and further in view of Ohtsuka (United States patent 5,388,100, issued February 7, 1995). The Applicants respectfully traverse the rejection.

As discussed above, Mahajan and Peace both fail to teach or suggest Applicants' invention where a component both processes serial data from a serial bit stream and selects a clock from among a plurality of clocks (*i.e.*, recovered clocks and a reference clock) to use for the processing of the serial data, as recited in the Applicants' independent claim 8. This deficiency is not bridged by the teaching of Ohtsuka.

Furthermore, claim 9 depends from independent claim 8 and recites additional features. Since Mahajan in view of Peace and further in view of Ohtsuka does not teach or suggest Applicants' invention as recited in independent claim 8, dependent claim 9 is also patentable and is allowable. Therefore, the Applicants contend that claims 8-9 are patentable over Mahajan in view of Peace and further in view of Ohtsuka and, as such, fully satisfy the requirements of 35 U.S.C. §103.

CONCLUSION

Thus, the Applicants submit that none of the claims presently in the application are obvious under the provisions of 35 U.S.C. §103. Consequently, the Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring issuance of an adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Thomas George at 408-879-4682 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent & Trademark Office on March 23, 2009.
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